

PHN103T

N-channel enhancement mode field-effect transistor

Rev. 02 — 28 April 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- TrenchMOS™ technology
- Low on-state resistance
- Fast switching
- Logic level compatible.

1.3 Applications

- Motor driver
- Battery management
- Actuator driver
- High speed, low resistance switch.

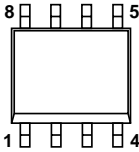
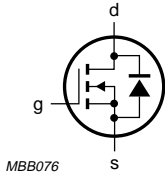
1.4 Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 4.5\text{ V}$	-	8.6	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$	-	6.25	W
T_j	junction temperature		-	150	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}$	20	30	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 2.5\text{ A}$	30	50	mΩ

2. Pinning information

Table 2: Pinning - SOT96-1 (SO8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	 <p>Top view MBK187</p>	 <p>MBB076</p>
4	gate (g)		
5,6,7,8	drain (d)		

SOT96-1 (SO8)



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3. Ordering information

Table 3: Ordering information

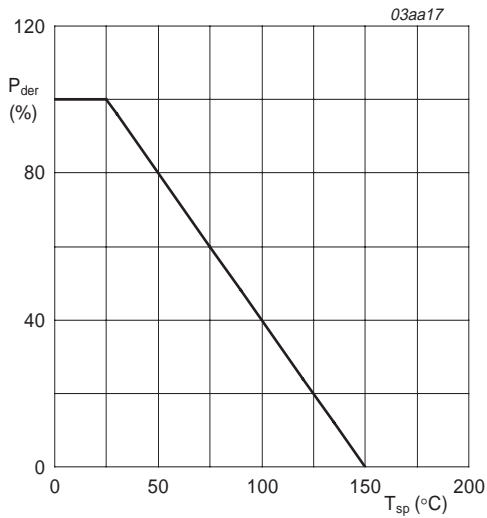
Type number	Package		Version
	Name	Description	
PHN103T	SO8	Plastic small outline package; 8 leads	SOT96-1

4. Limiting values

Table 4: Limiting values

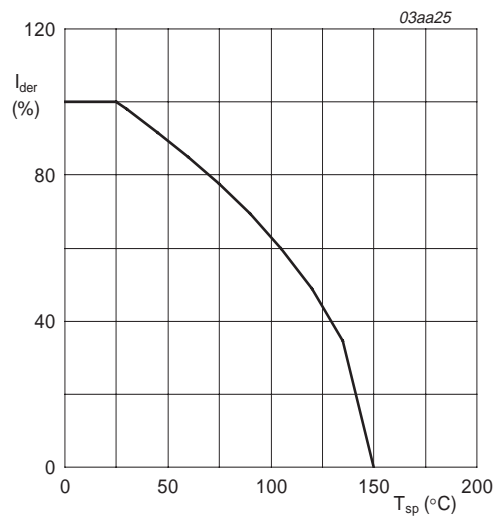
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{sp} = 25\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2 and 3	-	8.6	A
		$T_{sp} = 100\text{ °C}$; $V_{GS} = 4.5\text{ V}$; Figure 2	-	5.4	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	34	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; Figure 1	-	6.25	W
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-65	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	7	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	34	A



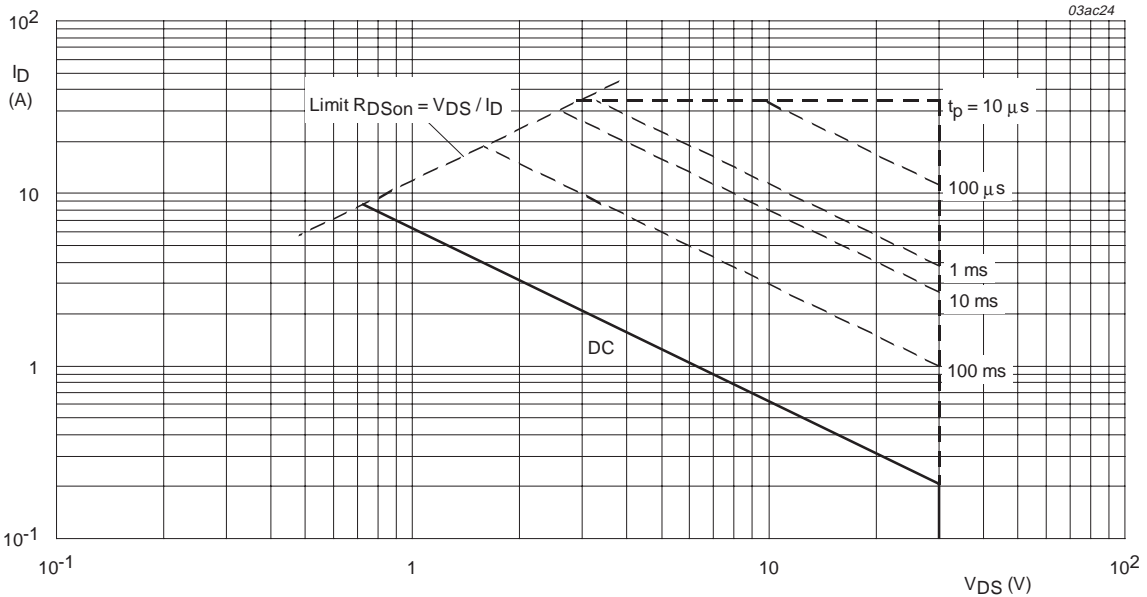
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



T_{sp} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	20	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	150	-	K/W

5.1 Transient thermal impedance

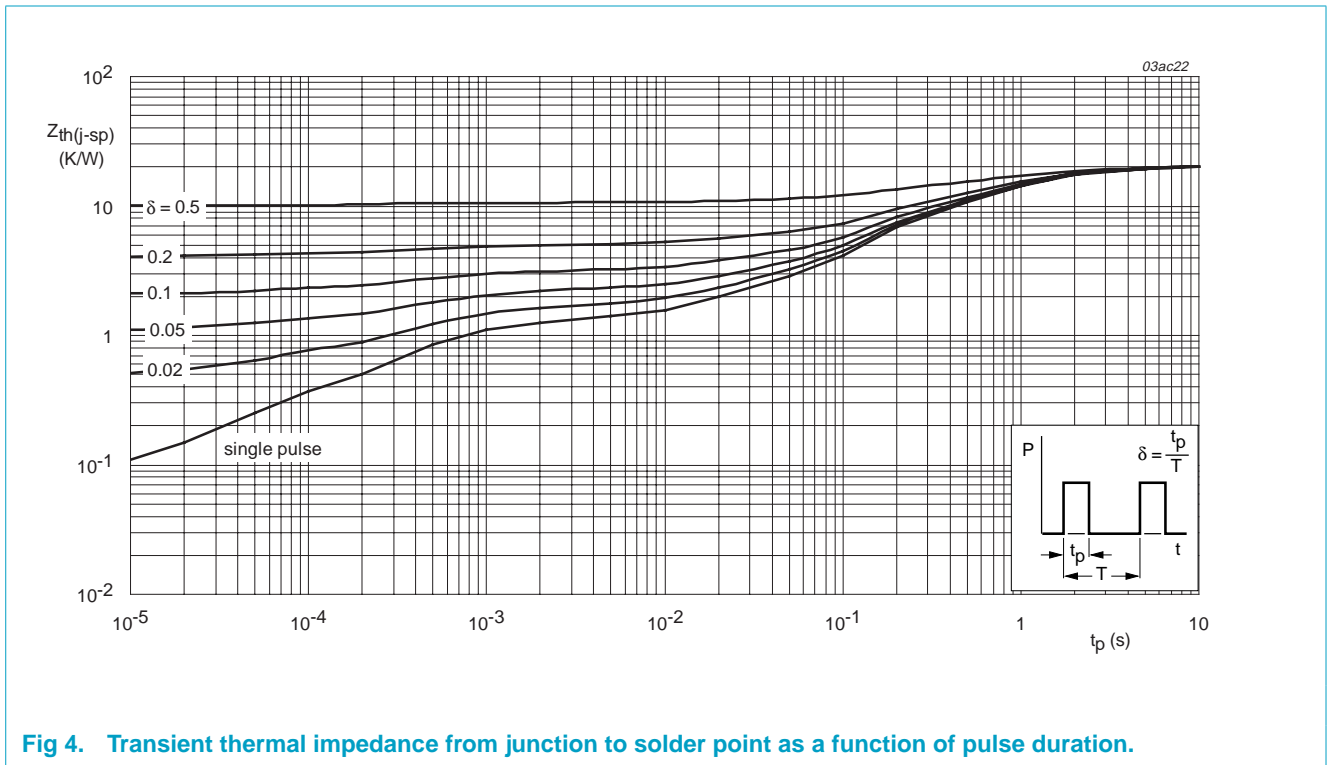
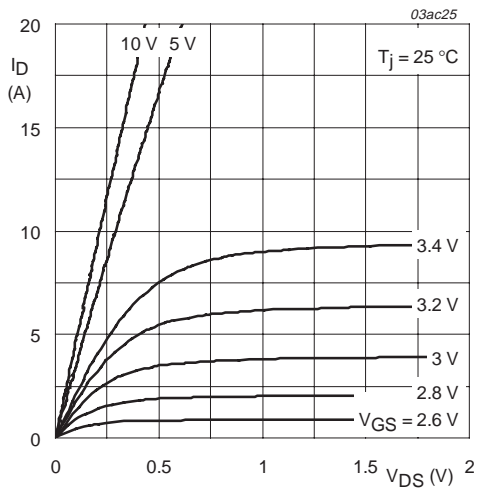


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

6. Characteristics

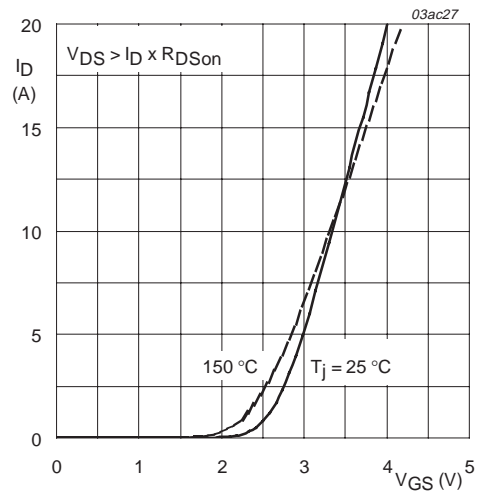
Table 6: Characteristics
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ }^\circ\text{C}$	30	43	-	V
		$T_j = -55\text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9 $T_j = 25\text{ }^\circ\text{C}$	1	2	2.8	V
		$T_j = 150\text{ }^\circ\text{C}$	0.6	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	-	-	3.5	V
I_{DSS}	drain-source leakage current	$V_{DS} = 24\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ }^\circ\text{C}$	-	10	100	nA
		$T_j = 150\text{ }^\circ\text{C}$	-	-	10	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 5\ \text{A}$; Figure 7 and 8 $T_j = 25\text{ }^\circ\text{C}$	-	20	30	m Ω
		$V_{GS} = 4.5\ \text{V}$; $I_D = 2.5\ \text{A}$; Figure 8 $T_j = 25\text{ }^\circ\text{C}$	-	30	50	m Ω
		$T_j = 150\text{ }^\circ\text{C}$	-	-	85	m Ω
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 5\ \text{V}$; $I_D = 5.5\ \text{A}$; Figure 11	-	12	-	S
$Q_{g(tot)}$	total gate charge	$I_D = 5\ \text{A}$; $V_{DS} = 15\ \text{V}$; $V_{GS} = 10\ \text{V}$; Figure 14	-	24	40	nC
Q_{gs}	gate-source charge		-	3.3	-	nC
Q_{gd}	gate-drain (Miller) charge		-	7.4	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 24\ \text{V}$; $f = 1\ \text{MHz}$; Figure 12	-	770	-	pF
C_{oss}	output capacitance		-	265	-	pF
C_{rss}	reverse transfer capacitance		-	180	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\ \text{V}$; $R_D = 15\ \Omega$; $V_{GS} = 10\ \text{V}$; $R_G = 6\ \Omega$	-	8	-	ns
t_r	rise time		-	10	-	ns
t_{on}	turn-on time		-	18	35	ns
$t_{d(off)}$	turn-off delay time		-	24	-	ns
t_f	fall time		-	20	-	ns
t_{off}	turn-off time		-	44	150	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 1.25\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 13	-	0.73	1.0	V
t_{rr}	reverse recovery time	$I_S = 1.25\ \text{A}$; $di_S/dt = -100\ \text{A}/\mu\text{s}$;	-	120	-	ns
Q_r	recovered charge	$V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$	-	150	-	nC



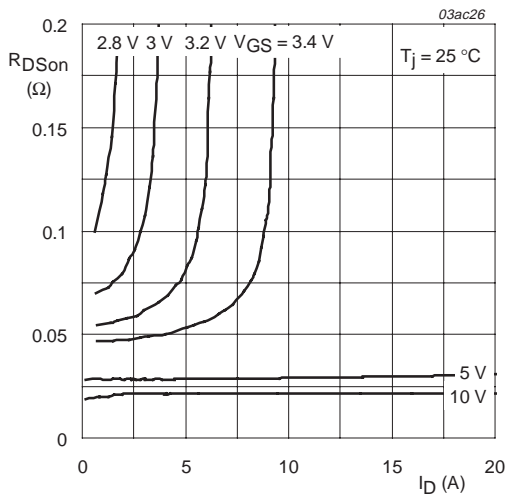
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



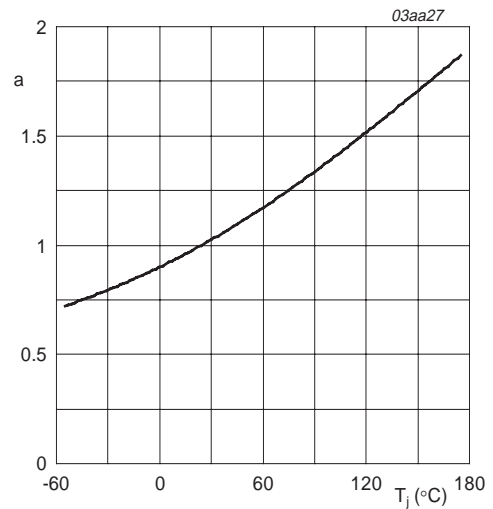
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



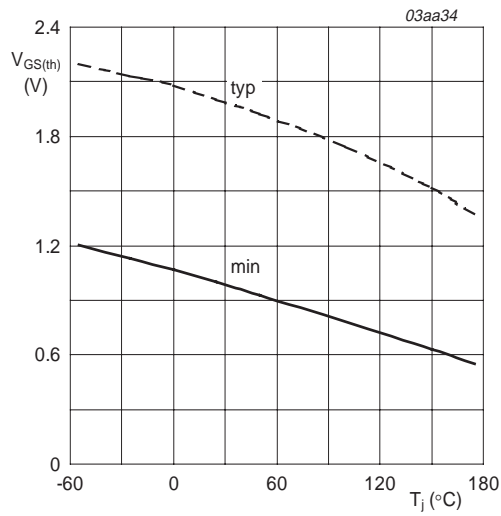
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



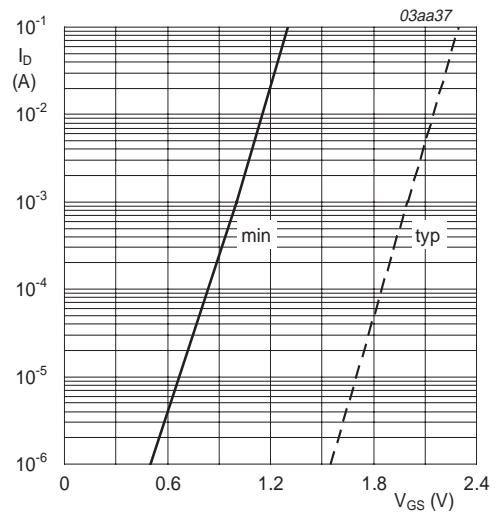
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



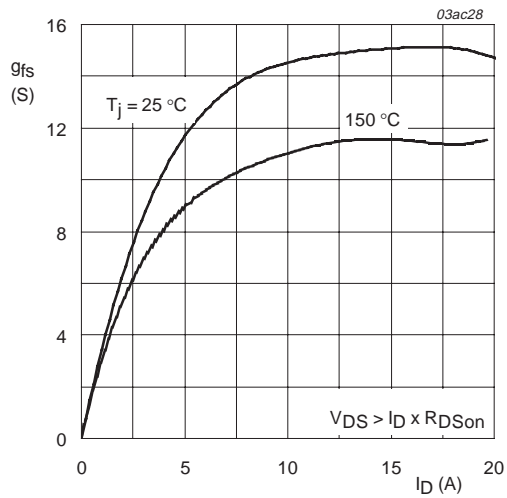
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



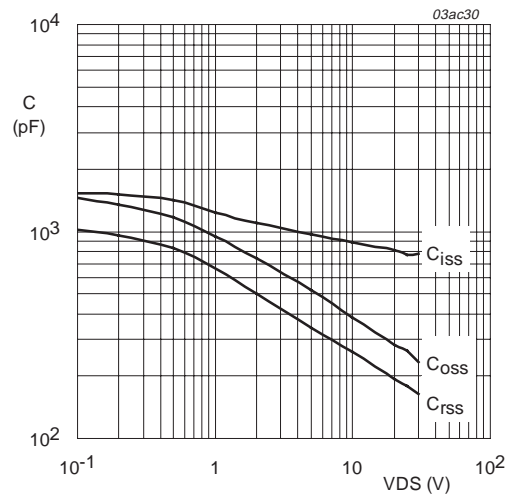
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



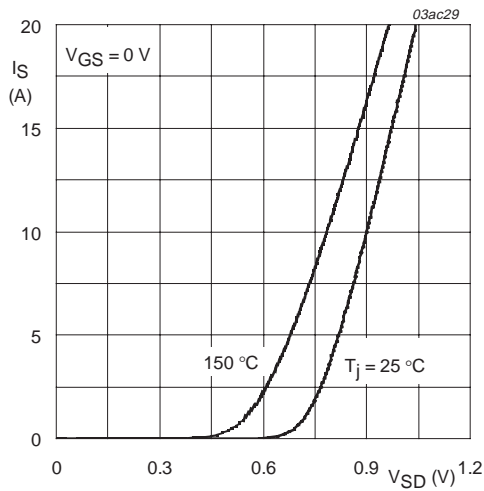
$T_j = 25 \text{ }^\circ\text{C}$ and $150 \text{ }^\circ\text{C}; V_{DS} > I_D \times R_{DS(on)}$

Fig 11. Forward transconductance as a function of drain current; typical values.



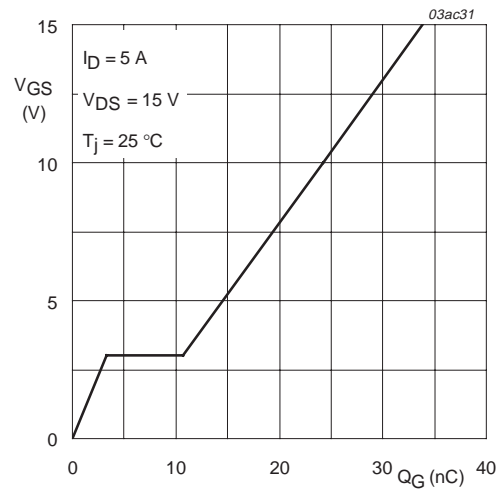
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0$ V

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 5$ A; $V_{DS} = 15$ V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

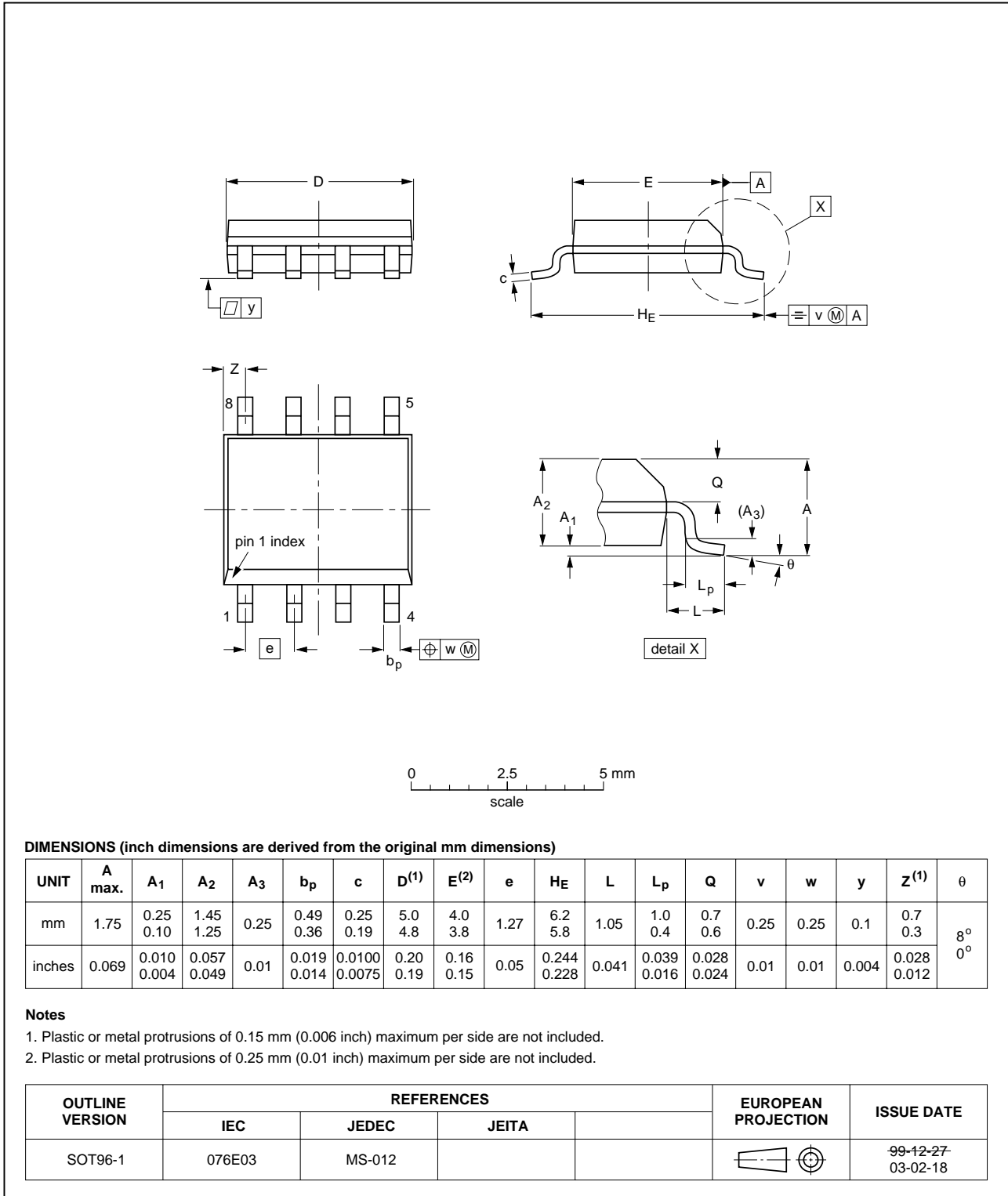


Fig 15. SOT96-1 (SO8).

8. Revision history

Table 7: Revision history

Rev	Date	CPCN	Description
02	20040428	-	Product data (9397 750 13185) Modifications <ul style="list-style-type: none">• Updated to latest standard.• Section 3 "Ordering information" added.• Section 6 "Characteristics" R_{DSon} conditions corrected.
01	20000828	HZG336	Product specification (9397 750 07304) Converted from VDMOS (Nijmegen) to TrenchMOS™ technology (Hazel Grove).

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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